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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,230	11/26/2003	Hidenori Sato	501.39288CX1	5683

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EXAMINER	
SMOOT, STEPHEN W	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 07/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/721,230	SATO ET AL.	
	Examiner	Art Unit	
	Stephen W. Smoot	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003 and 10 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) *1-9,13,16-20,22-24 and 29-41* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-12,14,15,21 and 25-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/709,403.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11-26-03; 2-10-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to application papers filed on 26 November 2003, which includes a preliminary amendment, and to applicant's election filed on 10 February 2005.

Election/Restrictions

1. Applicant's election of Group VI (claims 10-12, 14, 15, 27) and Group XI (claims 21, 25, 26, 28) in the reply filed on 10 February 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Accordingly, claims 1-9, 13, 16-20, 22-24, 29-41 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected species, there being no allowable generic or linking claim.

Information Disclosure Statement

2. The Korean document cited in the information disclosure statement filed on 26 November 2003 has not been considered because a copy of the document is not

present in the parent application (09/709,403). The other lined through documents are duplicate entries.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Semiconductor Integrated Circuit Device With a Trench Formed Between Adjacent Patterns that is Filled With Two Insulating Films and Its Method of Manufacture.

4. The disclosure is objected to because of the following informality:

Update the "Cross Reference" section (see preliminary amendment) to indicate that 09/709,403 has issued as US 6,693,008.

Appropriate correction is required.

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

6. Claim 26 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim, or amend the claim to place the claim in proper dependent form, or rewrite the claim in independent form.

The further limitation to claim 25 as set forth in claim 26 has also been set forth in the parent claim, claim 21 (see lines 5-6).

7. Claim 14 is objected to because of the following informality:

In claim 14, line 2, change "first insulating film" to --trench-- for proper antecedence to claim 10, step (b).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 10, 14, 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Andideh et al. (US 5,270,264).

Referring to Fig. 13 and column 4, line 4 to column 6, line 26, Andideh et al. disclose a semiconductor structure that includes metal lines (50) (i.e. patterns) formed on a semiconductor wafer (52) with two ILD layers (70, 100) used to fill gaps between adjacent metal lines (50). Both ILD layers are preferably deposited by PECVD (i.e. a chemical vapor deposition method. The first ILD layer (70) partially fills the gap and the second ILD layer fills the remainder of the gap as shown in Fig.13. These are all of the limitations set forth in claim 21 of the applicant's invention.

Referring to Figs. 2, 8-13 and column 4, line 4 to column 6, line 26, Andideh et al. disclose a method of forming a semiconductor structure that includes forming metal lines (50) (i.e. patterns) on a semiconductor wafer (52) and filling the gaps between adjacent metal lines (50) by depositing a first CVD ILD layer (70) to partially fill the gaps (step 20 in Fig. 2), sputter etching the first CVD ILD layer (70) to remove bread-loaf edge portions (72 in Figs. 11, 12) of the first CVD ILD layer (70) which is redeposited in the gaps (step 22 in Fig. 2), and depositing a second CVD ILD layer (100) to fill the remainder of the gaps (step 24 in Fig.2). These are all of the limitations set forth in claims 10, 14 of the applicant's invention.

10. Claims 10, 14, 15, 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Yabu et al. (US 5,960,300 – from applicant's IDS filed on February 10, 2005).

Referring to Figs. 9(a)-9(f) and column 20, line 16 to column 21, line 35, Yabu et al. disclose a method of forming trench isolation structures that includes patterning a silicon dioxide film (11) and a polysilicon film (22) with photoresist to etch trenches (10a) into a semiconductor substrate (10) (also see Fig. 1(a)). The trenches (10a) are then filled with a reflowable insulating film (34) as shown in Fig. 9(a), which is subsequently reflowed by a thermal treatment to eliminate voids (19) as shown in Fig. 9(b). The reflowable insulating film (34) is then etched back to form buried layers (34a) at the bottom of the trenches as shown in Fig. 9(c) and the remainder of the trenches (10a) are filled with another insulating film (31) as shown in Fig. 9(d). The second insulating film (31) is silicon dioxide, which can be deposited by CVD (i.e. chemical vapor deposition) (also see column 9, lines 50-55). These are all of the limitations set forth in claims 10, 14, 15 of the applicant's invention.

Regarding claim 21, Fig. 9(f) shows a trench isolation structure that includes trenches (10a) formed in etched (i.e. patterned) portions of a semiconductor substrate (10 in Fig. 1(a)) that is filled with a buried reflowable insulating film (34a in Fig. 9(e)) and an overlying insulating film (31a in Fig. 9(e)) that can be silicon dioxide formed by CVD (also see column 9, lines 50-55). These are all of the limitations set forth in claim 21 of the applicant's invention.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 11-12, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andideh et al. (US 5,270,264) as applied to claim 10 above and Claims 25-26, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andideh et al. (US 5,270,264) as applied to claim 21 above, and further in view of Kuroi et al. (US 6,218,262 B1).

As shown above, Andideh et al. anticipate claims 10 and 21 of the applicant's invention. Andideh et al. also anticipate the further limitation to claim 11 as set forth in claim 12 of the applicant's invention, which is to deposit the second insulating film by CVD. Further, as indicated above, claim 26 does not further limit claim 25.

However, Andideh et al. lack the further limitations to claim 10 as set forth in claims 11, 27, which are the plurality of patterns including a gate electrode and a dummy electrode (claim 11) and the plurality of patterns being dummy patterns in an isolation trench (claim 27). Further, Andideh et al. lack the further limitations to claim 21 as set forth in claims 25, 28, which are the plurality of patterns including a gate

electrode and a dummy electrode (claim 25) and the plurality of patterns being dummy patterns in an isolation trench (claim 28).

Referring to Fig. 17 and column 17, line 20 to column 20, line 62, Kuroi et al. teach a DRAM structure that includes patterns of dummy gate electrodes (14A, 14D) and gate electrodes (14B, 14C) formed on a silicon substrate (1) with an inter-layer insulation film (18) formed over and between these electrodes (14A, 14B, 14C, 14D). The dummy gate electrode (14A) is formed in an isolation trench (10A).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Andideh et al. and Kuroi et al. in order to use two insulating layers, as taught by Andideh et al., as the inter-layer insulation film of Kuroi et al. Andideh et al. recognize that their gap filling method, which features a sputter etching step between the steps of depositing the two insulating layers, has the advantage of completely filling gaps between metal lines (e.g. gate lines) (see column 9, lines 4-17).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Harvey teaches gap filling of an interconnect structure that includes dummy patterns.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sws

Stephen W. Smoot

STEPHEN W. SMOOT
PRIMARY EXAMINER